Unit / Module Name:	
Unit / Module Number:	SHB
Used On:	TIM modules
Document Issue:	See Revision history table
Date:	See Revision history table

CONFIDENTIAL

Specifications of the Sundance High-speed Bus Standard.

Approvals		Date
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Certificate Number FM 55022

Revision History

	Changes Made	Issue	Initials
02.05.02	**First issue.**	**1.0**	**E.P**
14.02.03	**Addition in paragraph 5.3 of warning about restrictions on Virtex II clock and routing resources. See** Xilinx Answer Record #11756. **Addition in 6.1 of Web link to Inter Module SHB connections.** **Correction in 6.2.1 of the configuration code 043850060010GG20 which is incorrect to the configuration code 043850060010JM20.**	**1.1**	**E.P**
21.02.03	**Recommended connector placement-Figure 4 modified to match Sundance placement on TIM Modules.**	**1.2**	**E.P**
09.06.03	**SHB word configuration pinout modified to be able to match 2xhalf-word interfaces pinout. Replaced linked drawings by embedded drawings.**	**1.3**	**E.P**
12.06.03	**General update to eliminate confusions on terminology between SDB interface/Hw SHB interface and W SHB Interface. More detailed explanations about which interface is compatible with which.**	**1.4**	**E.P**

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1 SHB (Sundance High-speed Bus)

1.1 Related Documents

Sundance SDB specification.

TI TIM specification & user's guide.

Samtec QSH Catalogue page

1.2 Overview

The following specifications provide a framework for SHB (Sundance High speed Bus) communication.

SHB is SUNDANCE new communication standard for data transmission applications. The standard is based on the Sundance Digital Bus (SDB) developed by SUNDANCE and extends it to provide a more performing technology. For years, SUNDANCE and its customers have successfully used the SDB standard method of communication. Both SUNDANCE and its customers developed products (motherboards, TIM modules, see TI TIM specification & user's guide) with SDB connectivity and the SDB FPGA design interface and realized the necessity to keep on sharing the same standard as making cables, selecting connectors, using incompatible voltage levels could become very confusing and very costly otherwise.

As data rates and FPGA pin numbers continue to increase, it becomes necessary to provide a new standard that will remain compatible with the SDB standard, also will provide faster communications, will make use of a higher density of pins per FPGA and connector, and will reliably transmit on long distances.

The standard link will be able to handle the increased signal speeds, and the cable assembly will allow customers to communicate between boards providing SHB or SDB.

The boards on which the SHBs will be provided are TIM modules. More information can be found at: TI TIM specification & user's guide.

1.3 Single Ended Transmission

The LVTTL standard is the supported standard for the SDB/SHB.

The Low-Voltage TTL, or LVTTL standard is a general purpose single-ended standard for 3.3V applications.

Single-ended transmission is performed on one signal line, and the logical state is interpreted with respect to ground.

Although it is possible to make it 5V compliant the SHB standard is dependant on the FPGA implementing the interface. Therefore to comply with the latest technology in FPGAs the SHB interface is 3.3V but NOT 5V tolerant.

Figure 1 shows the electrical schematic diagram of a single-ended transmission system.

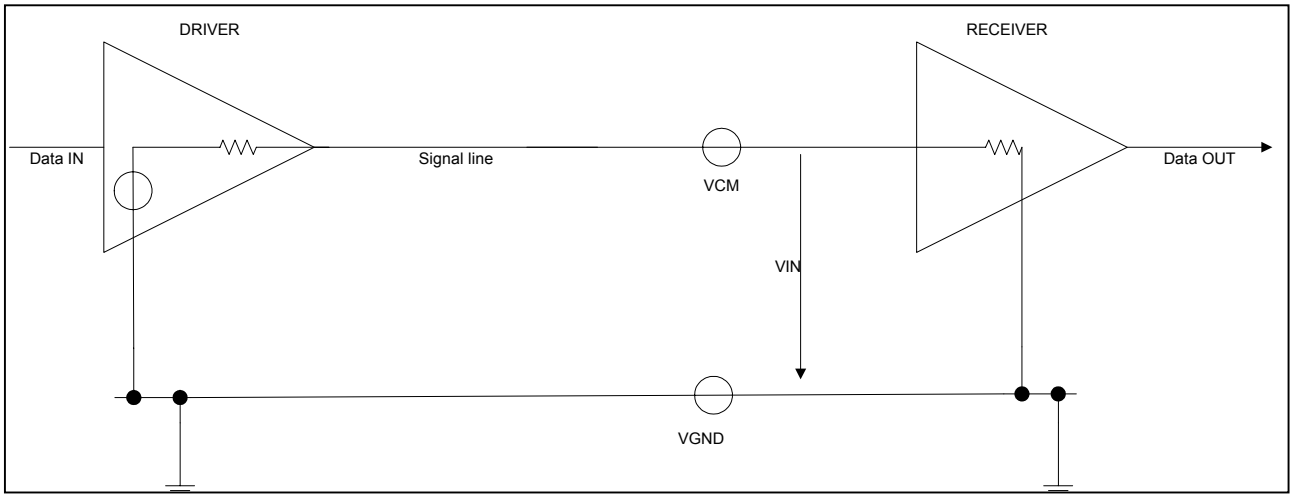

Figure 1: Single ended transmission

PARAMETER	MIN	MAX	UNITS
V_{IH}-High level input voltage	2	$V_{DD+0.3}$	V
V_{IL} High level input voltage	-0.3	0.8	V
I_{IN} input current		±5	uA
V_{OH} High level output voltage	2.4		V
V_{OL} High level output voltage		0.4	V

Table 1: Standard LVTTL switching levels

3.3 V nominal supply: V_{DD}(min) = 3.0 V and V_{DD}(max) = 3.6 V-normal range

1.4 Technology Benefits

1.4.1 Low pin count

A single-ended system requires only one line per signal for short distances and low frequencies.

The Sundance Digital Buses (SDB) featuring high speeds signals require a single ground return path for each signaling line on a ribbon cable, using a total of 2 pins/connector/signal.

However, the Sundance High-speed Buses (SHB) eliminate the need of having 2 lines per signal by using Micro-coax ribbon cables or flexi-PCBs instead of a traditional ribbon cable and bring down the pin count to 1 pin/connector/signal.

1.4.2 High data transfer rate

The Sundance Digital Buses (SDB), allow a maximum frequency of 100Mhz; but the faster Sundance High Speed Buses featuring higher speeds signals allow a maximum theoretical frequency in excess of 200Mhz.

2 Sundance High-speed Bus FPGA Interfaces

This section provides definitions for the signals used in the SHB Interfaces and their configurations.

The SHB interfaces come under three different configurations differentiated by the size of the data bus.

But first, a quick reminder on the SDB interface protocol and signals which the SHB Interfaces are based on.

2.1 SDB Interface

Sundance developed the SDB technology as a solution for fast data transfers, based on LVTTL.

The Sundance Digital Bus (SDB) was developed as a mean to allow data to be transmitted or received at rates in excess of 100 Mbytes/s.

The SDB Interface transfers 32-bit words in two clock cycles and stores two 16-bit data received into a 32-bit word FIFO ready to be used.

The transmission can be fully BI-DIRECTIONAL.

An SDB transmission occurs between a transmitter and a receiver pair.

The transmitter accepts 16-bit single ended data, a single ended clock, a single ended Enable signal and 2 single ended signals handling the bus exchange.

A 16-bit data is transmitted in parallel at each clock cycle when WEN is Low.

Each signal is ground interlaced.

The receiver accepts the 16-bit LVTTL data stream, the clock, the Enable signal, and the 2 signals that control the bus exchange.

A more detailed explanation can be found at: SDB.

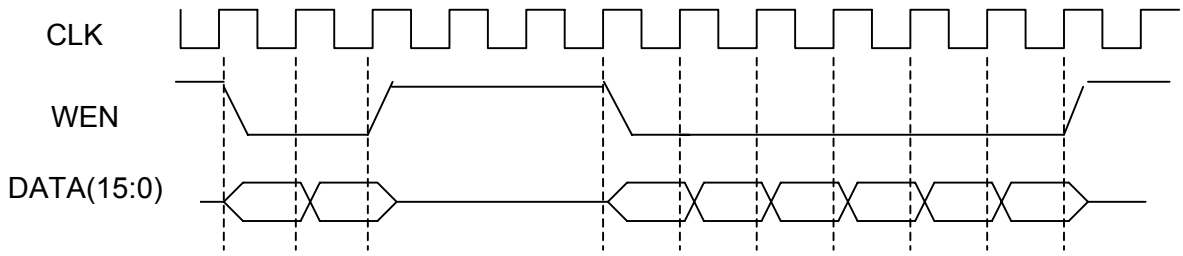

Figure 2: Timing Diagram of the Data Transmission

2.2 SHB Interface signals definitions

The SHB interfaces use the same protocol as the SDB interface protocol.

Therefore, the SHB interfaces data, enable and controls are transmitted on the same bus.

One enable signal is defined as:

- WEN: Write Enable is defined LOW for valid data.

Two control signals are defined as:

- REQ: Bus request is defined HIGH by the receiver for a Bus exchange request.
- ACK: Bus Acknowledge is define HIGH by:
  - The transmitter to answer a bus request and acknowledge the bus.
  - The receiver to hold a transmission in case of its FIFO is almost FULL FIFO.

One clock signal:

- CLK.

Four User-defined signals are defined as:

- USERDEF0: spare
- USERDEF1: spare
- USERDEF2: spare
- USERDEF3: spare

Users can define these signals to meet their needs for a particular product.

2.3 Bus Configurations

The SHB interfaces come under three different configurations differentiated by the size of the data bus.

The naming conventions for the various configurations are:

• Byte: 8-bit data Bus: D[0:7].

• Half-word: 16-bit data Bus: D[0:15]. (same data bus size as for a SDB interface)

• Word: 32-bit data Bus: D[0:31]

The most recent TIM modules from Sundance allow to select between 2 Hw interfaces or 1 Word interface per connector.

Please refer to the User Manual of your module to find out which configuration is available and how many interfaces per connectors are available. Most of our modules implement 2 Hw SHB interfaces per connector and don’t implement any Byte SHB interface.

2.3.1 Byte Configuration

CLK
D0
D1
D2
D3
D4
D5
D6
D7
WEN
REQ
ACK

Table 2: Byte Configuration

2.3.2 Half-word Configuration

CLK
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
USERDEF0
USERDEF1
USERDEF2
USERDEF3
WEN
REQ
ACK

Table 3: Half-word Configuration

You can notice that this configuration provides the same amount of data lines as an SDB interface. Therefore an SDB interface and a Hw SHB interface are fully compatible.

As a result, modules with an SDB interface can communicate with module with a Hw SHB interface.

2.3.3 Word Configuration

Table 4: Word Configuration

3 SHB Connections

3.1 QSH-30 Connector

The following describes the SAMTEC 60-pin connector (QSH series) selected for the SHB communications, to be populated **on the board**.

Features:

- High-speed socket strip: SAMTEC **QSH-030-01-L-D-A-K** on the board
- Centreline: 0.5mm (0.0197”)
- http://www.samtec.com/ftppub/pdf/QSH.PDF

The advantage of this connector is that it can sustain high-speed operation thanks to controlled impedance and an active shielding (central ground blade).

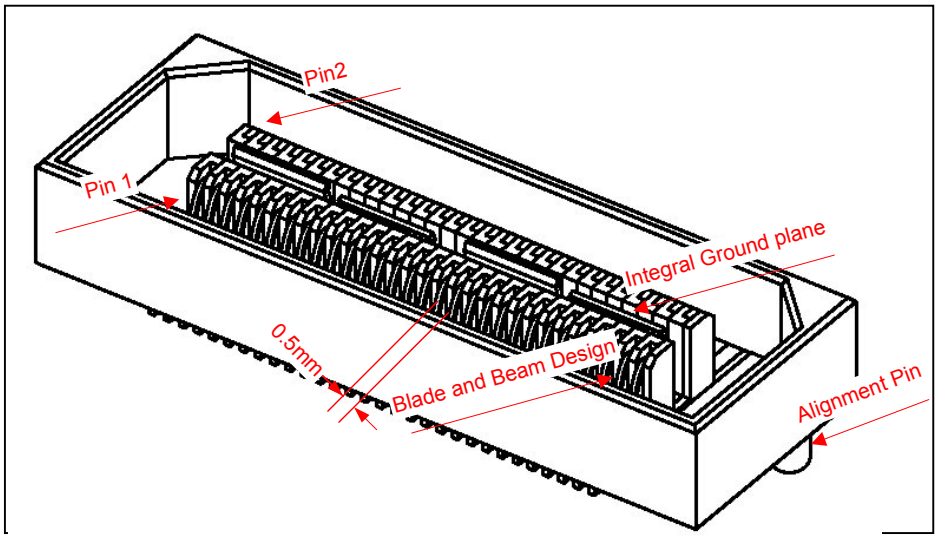

Figure 3: QSH 30

3.2 Pin Number Orientation

1	2
3	4
5	6
7	8
…	…
59	60

Table 5: Connector Pin Numbering

3.3 Configuration

The connector can support up to

- 5 Byte configurations SHB interfaces or
- 2 Half-word + 1 Byte configurations SHB interfaces or
- 1 Word configuration SHB interface.

Configuration	Naming convention	Configurations per connector
Byte	B	B0, B1, B2, B3, B4
Half-word	Hw	Hw0, B2, Hw1
Word	W	W

Table 6: Configurations Assignment per Connector

All the tables will follow the following colour pattern:

32-bit Interface
16-bit interface
8-bit interface

The most recent TIM modules from Sundance allow to select between 2 Hw interfaces or 1 Word interface per connector.

Please refer to the User Manual of your module to find out which configuration is available and how many interfaces per connectors are available. Most of our modules implement 2 Hw SHB interfaces per connector and don't implement any Byte SHB interface.

3.4 Sundance High Speed Bus Board Connector Pinout

W		Hw		B	QSH Pin number	QSH Pin number	W		Hw		B
CLK	Hw0	CLK	B0	CLK	1	31			D5	B2	D5
D0		D0		D0	2	32			D6		D6
D1		D1		D1	3	33			D7		D7
D2		D2		D2	4	34			WEN		WEN
D3		D3		D3	5	35			REQ		REQ
D4		D4		D4	6	36			ACK		ACK
D5		D5		D5	7	37		Hw1	CLK	B3	CLK
D6		D6		D6	8	38	D16		D0		D0
D7		D7		D7	9	39	D17		D1		D1
D8		D8		WEN	10	40	D18		D2		D2
D9		D9		REQ	11	41	D19		D3		D3
D10		D10		ACK	12	42	D20		D4		D4
D11		D11	B1	CLK	13	43	D21		D5		D5
D12		D12		D0	14	44	D22		D6		D6
D13		D13		D1	15	45	D23		D7		D7
D14		D14		D2	16	46	D24		D8		WEN
D15		D15		D3	17	47	D25		D9		REQ
		USERDEF0		D4	18	48	D26		D10		ACK
		USERDEF1		D5	19	49	D27		D11	B4	CLK
		USERDEF2		D6	20	50	D28		D12		D0
		USERDEF3		D7	21	51	D29		D13		D1
WEN		WEN		WEN	22	52	D30		D14		D2
REQ		REQ		REQ	23	53	D31		D15		D3
ACK		ACK		ACK	24	54			USERDEF0		D4
		CLK	B2	CLK	25	55			USERDEF1		D5
		D0		D0	26	56			USERDEF2		D6
		D1		D1	27	57			USERDEF3		D7
		D2		D2	28	58			WEN		WEN
		D3		D3	29	59			REQ		REQ
		D4		D4	30	60			ACK		ACK

Table 7: Pin Assignment according to Configuration.

3.5 SHB Terminations

The termination is achieved by the FPGA. Some Pull ups/Pull downs are necessary:

Signal	Pull up/Pull down
WEN	Pull Up, 4K7
REQ	Pull Down, 4K7
ACK	Pull Down, 4K7

4 PCB Layout

The target board for the QSH connectors is a TIM module.

This module conforms to the TIM standard for single width modules. It requires an additional 3.3V power supply (as present on all Sundance TIM carrier boards), which must be provided by the two diagonally opposite mounting holes.

4.1 Recommended Connector placement and keep out area

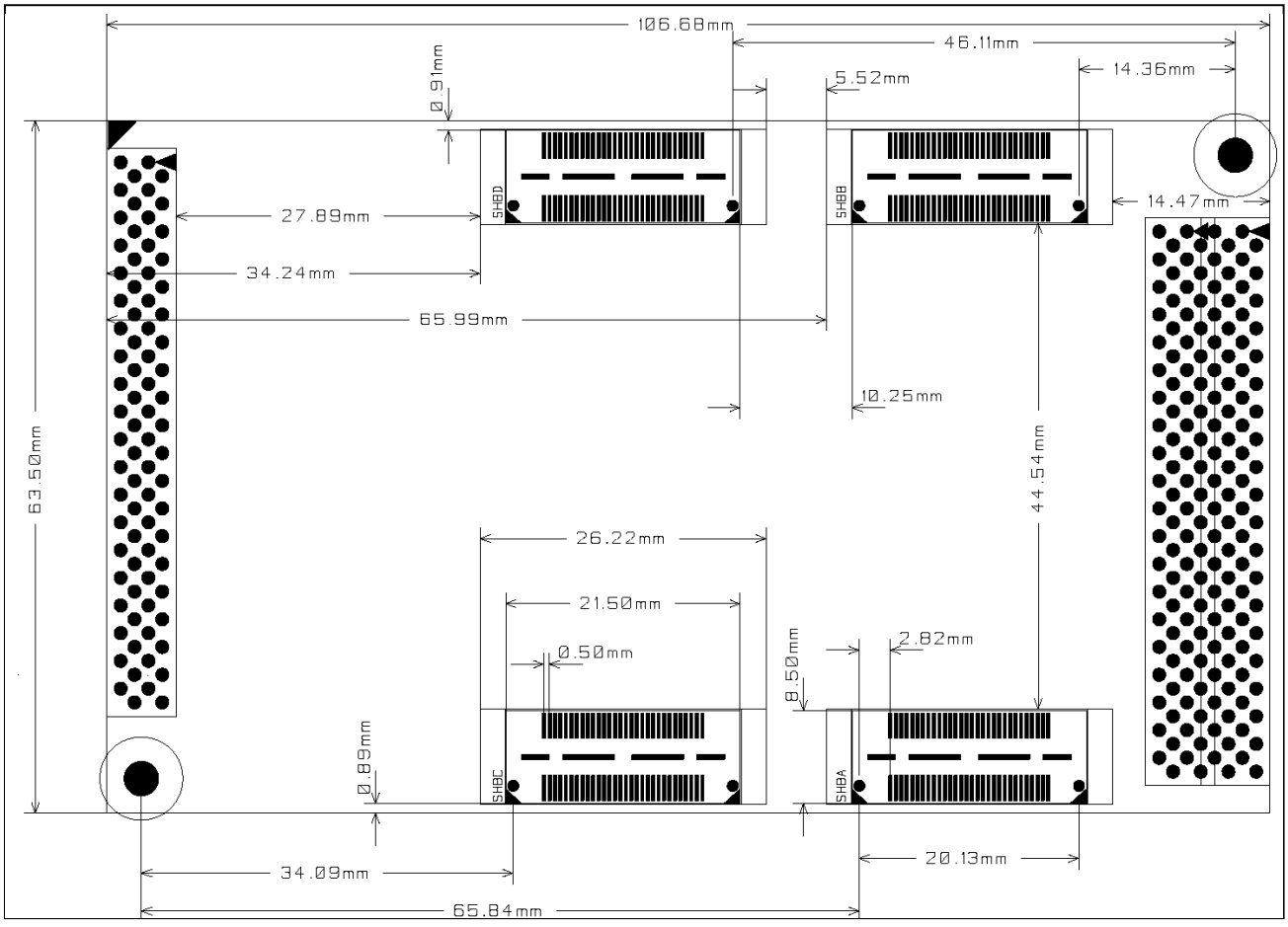

Figure 4: QSH placements on TIM module

The keep out area is 2.36 mm on each side of the QSH connector.

The naming convention for the connectors should be respected.

4.2 Recommended Connector Footprint dimensions

Figure 5 shows the board-layout for one connector (60-pin connector shown).

(All central divider pads should be tied to the ground plane)

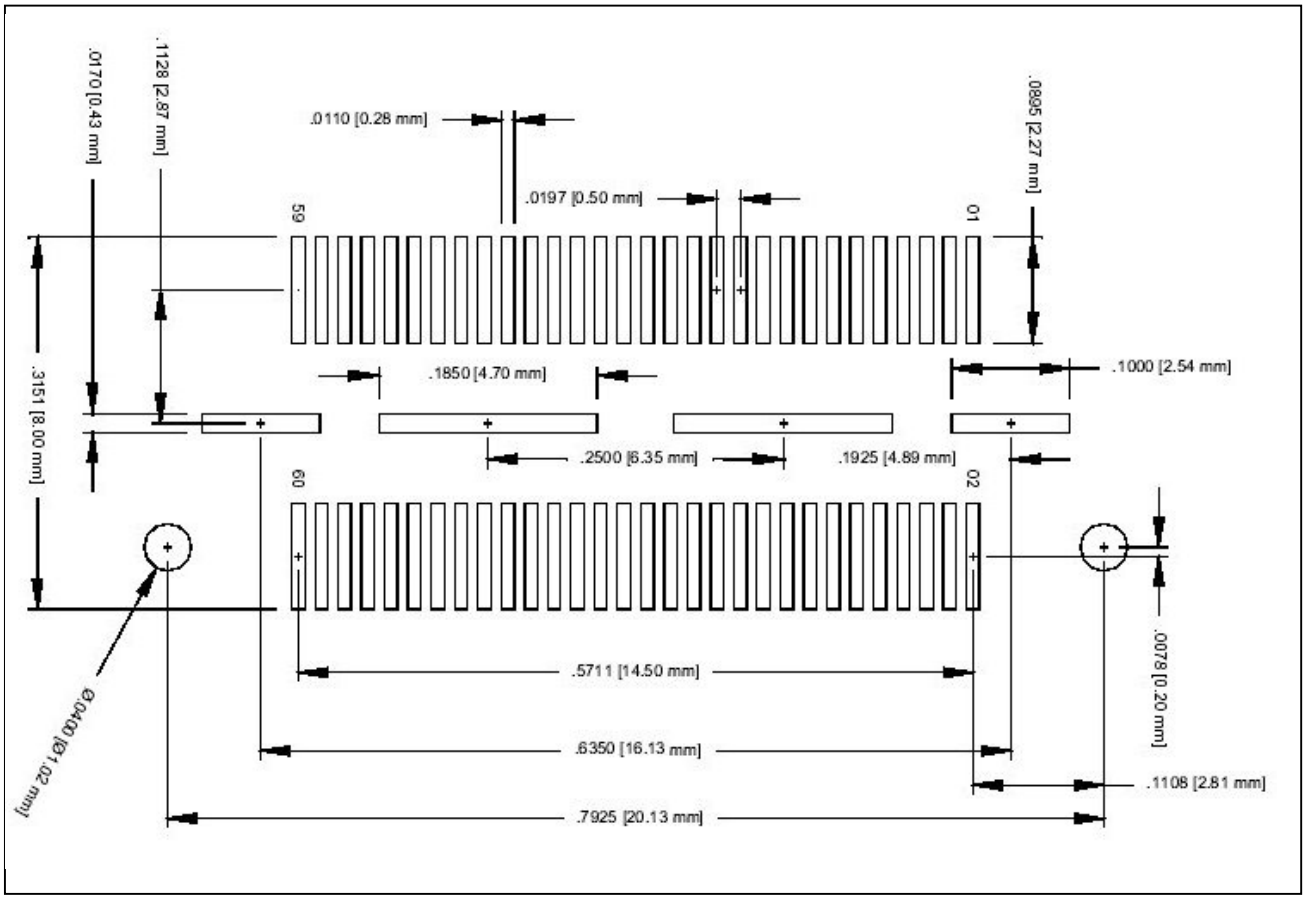

Figure 5: SAMTEC PN: QSH-030-01-L-D-A-K

5 FPGA connections

This part describes

5.1 Virtex II

The selected programmable device to host the SHB Interface is a XILINX FPGA from the Virtex II family.

5.2 IO Voltage

The I/O voltage MUST be LVTTL.

No termination is required on the lines.

5.3 Using Global Clock Networks in Virtex II

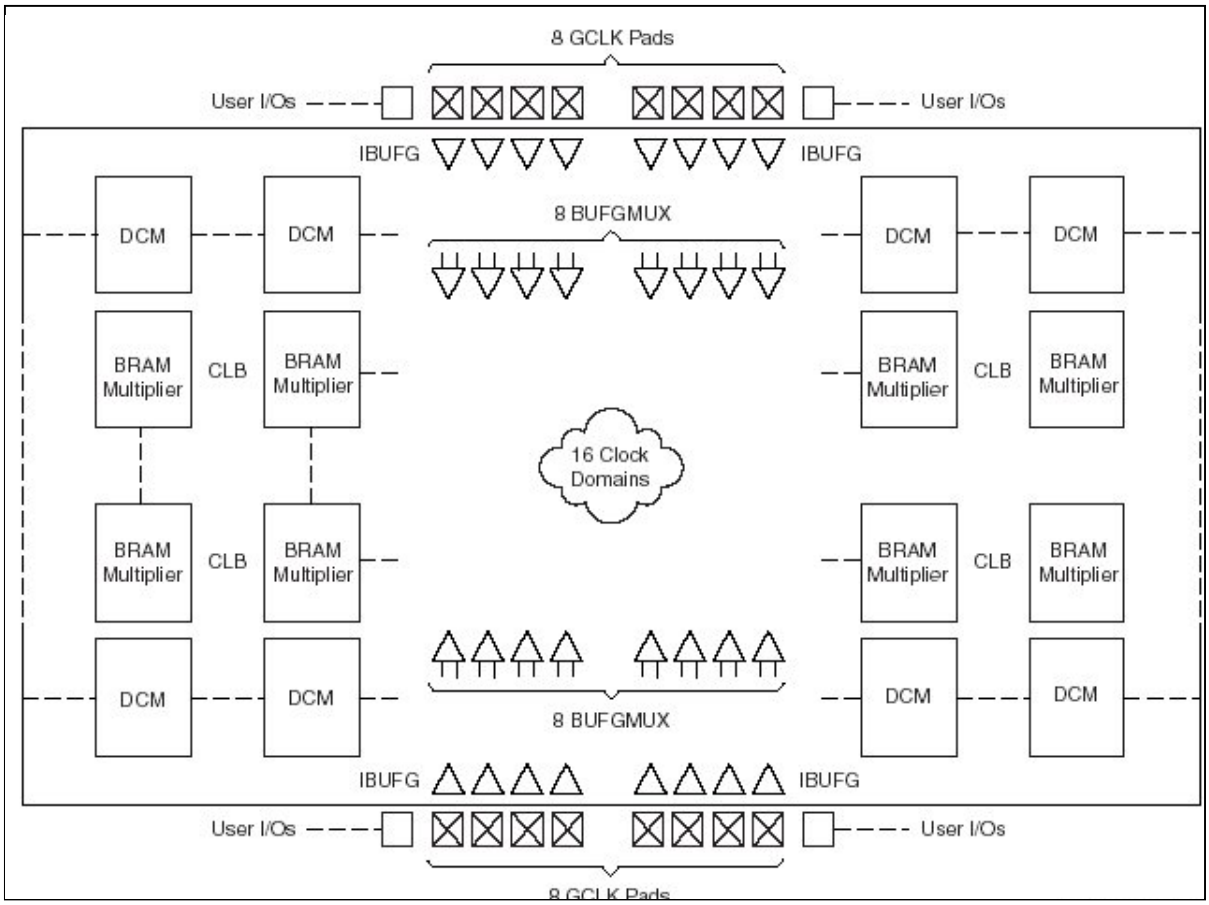

Figure 6: Clock resources in Virtex II devices

As the SHB interface is a very high frequency design, it is necessary to be able to benefit from the low-skew advanced clock distribution of the Virtex II devices.

It is then necessary to floorplan the SHB clock signals onto GCLK Pads of the Virtex II.

Only 2 of the SHB interface clock signals can be mapped onto any of the dedicated clock pads of these devices.

The reason is that the SHB Interface designs could instantiate any SHB configuration.

In the case of BYTE configurations being instantiated, all of the SHB clock signals could be mapped onto GCLK pads

In the case of Half-word configurations, only CLK0 and CLK3 are clock signals with CLK1, 2, 4 being data.

Therefore it is necessary not to map CLK1, 2, 4 clock signals on GCLK Pads as they would follow a different path in the chip than the rest of the data bus and they could be separated from the rest of the SHB Interface data bus.

In the case of a Word configuration, the same remark applies to CLK1, 2.

So, as a rule, **only map CLK0 and CLK3 onto GCLK Pads**

Xilinx Virtex II devices have restrictions on IBUFG, DCM, and BUFG routing.

Please follow the rules provided in Xilinx Answer Record #11756 to floorplan the SHB signals onto the Virtex II pins and ensure an optimal use of the Virtex Clock routing and resources.

5.4 FPGA Mapping of Sundance High-speed Bus Signals

Floorplanning of the FPGA pins should follow the orientation of the SHB connector on the board and avoid traces to cross each other.

5.4.1 Minimum SHB mapping

Depending on your requirements, It can happen that you are left with an amount of pins available on the FPGA lower than the 60 pins required to map a whole SHB connector.

In this case the minimum requirement is to map a **Half-word configuration** (See Table 3 and Table 7) onto your FPGA:

- **SHB A** and **SHB B** (see Figure 4): Map **W0**.
- **SHB C** and **SHB D** (see Figure 4): Map **W1**.

6 SHB link

6.1 QTH-30 Connector

- The following describes the SAMTEC 60-pin connector, QTH series, selected for the SHB communications **link**, mating connector of the QSH series fitted on the board.

  The QTHs are used on cable assembly, Flexi-PCBs or mezzanine boards.
  InterModule connections can be found at: Inter Module Connections

- Different heights are available in the QTH series.

LEAD STYLE: **0x**	Mating height with QSH
-01	(5,00) .197
-02	(8,00) .315
-03	(11,00) .433
-04	(16,00) .630
-05	(19,00) .748
-06	(22,00) .866
-07	(25,00) .984
-08	(30,00) 1,181

Table 8: QTH height selection

The board specifications MUST provide information concerning the SHB link required to connect on the QSH connectors of that board.

6.2 Cable

6.2.1 Standard Cable assembly

High-speed data transfer can be achieved between two SHB interfaces thanks to the use of the SHB cable assembly.

The standard cable assembly is composed of:

- A SAMTEC **QTH-030-0x-L-D-A-K** connector, mating with the onboard SAMTEC QSH connector.
- This connector comes in different heights, with the standard height being –01 (See Table 8)
- A 60-way flat ribbon micro-coax cable, 38 AWG, 50 Ohms.

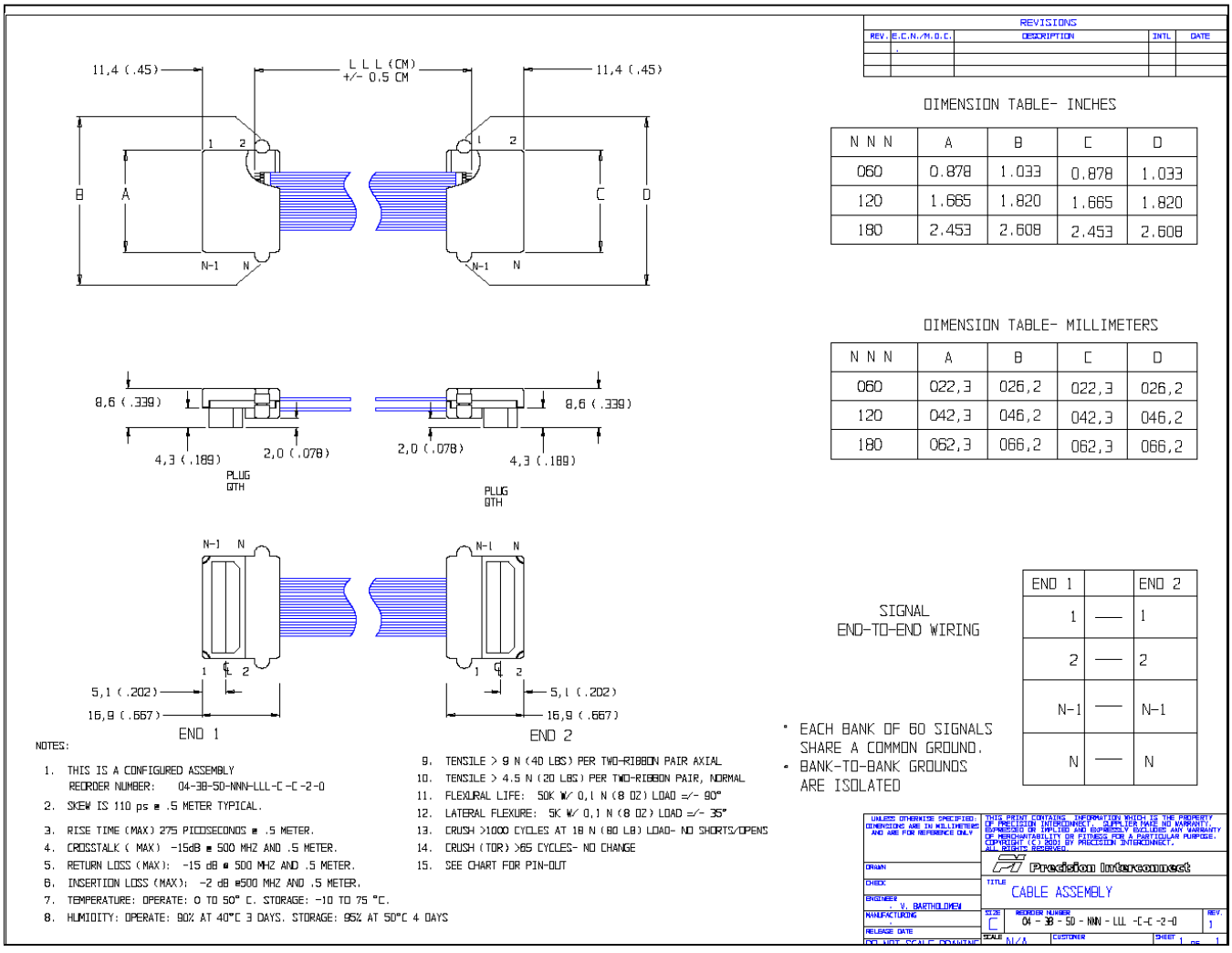

Figure 7: Standard Cable Assembly

The cable is custom made by Precision Interconnect and a standard cable assembly configuration is available at:

http://www.precisionint.com/tdibrsb/content/howtouse.asp

You need to enter the configuration code **043850060010JM20** in the configuration field in order to access the cable data.

Please note that this standard cable has been made as an example only, and you need to check whether your system needs a cable or could use PCB adaptors instead.

If you need more information or help, please contract Emmanuelp@sundance.com.

The next paragraphs refer to alternative ways of connecting SHB connectors to the outside world.

6.2.2 Custom cable assembly

In order to plug a cable on SHBC and SHBD (See Figure 4), the cable assembly must be able to overlap with components and meet the minimum height restriction on the board.

Likewise, plugging a cable onto SHBA and SHBB requires that the cable overlaps with an adjacent TIM module.

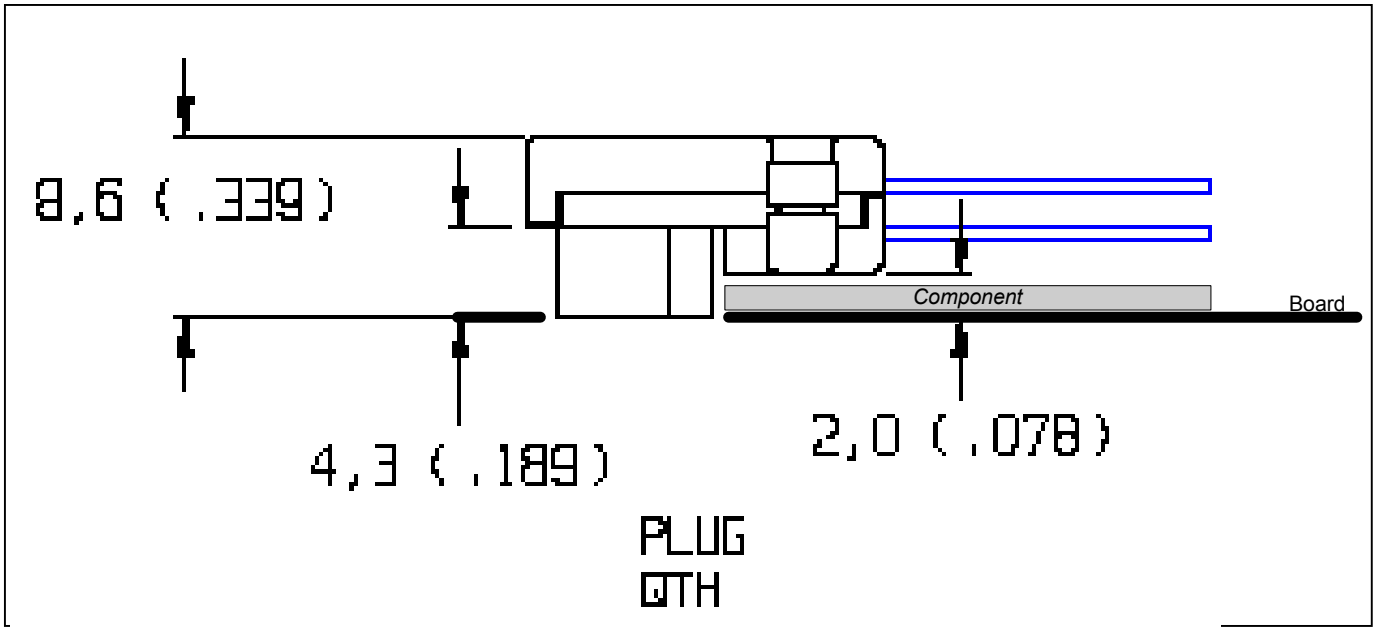

Figure 8: QTH connector height requirement

Therefore, in order to specify the correct construction for your application you must determine the QTH connector height requirement. To do so, please refer to QTH-30 Connector and to the board specification section entitled: SHB Link, found in the board User Manual and in the board specifications

Then use the solution builder found at: http://www.precisionint.com/tdibrsb/content/howtouse.asp

Go ahead and construct the cable you want using the standard height.

This will create the part number you need, an engineering drawing and give you all the performance data for the assembly.

Just specify the connector you want, for a different height version, in the **Questions or special requests** field of the order form

You can also get quotes on the page for quantities from 1 to 1,000 units.

7 SHB to SDB

Standard	SDB	SHB
Signals Voltage	LVTTL	LVTTL
Connector Pin count	SDB-Standard 20 pins used for bidirectional Interface (See Sundance SDB specification.)	Half-word Configuration 20 pins used for bidirectional Interface
Interface protocol	SDB protocol	SDB protocol
Board Connector	ODU 40-way socket	SAMTEC QSH-60 pins

The backward compatibility with the SDB standard is possible by fitting an adaptor on the QSH connector.

SDB Connector 0	SDB signal	SHB	Hw	SHB Connector
1	CLK	Hw0	CLK	1
3	D0		D0	2
5	D1		D1	3
7	D2		D2	4
9	D3		D3	5
11	D4		D4	6
13	D5		D5	7
15	D6		D6	8
17	D7		D7	9
19	D8		D8	10
21	D9		D9	11
23	D10		D10	12
25	D11		D11	13
27	D12		D12	14
29	D13		D13	15
31	D14		D14	16
33	D15		D15	17
35	USERDEF0		USERDEF0	18
37	WEN		WEN	22
38	REQ		REQ	23
39	USERDEF1		USERDEF1	19
40	ACK		ACK	24
			USERDEF2	20
			USERDEF3	21

SDB Connector 1	SDB		Hw	SHB Connector
1	**CLK**	Hw1	**CLK**	37
3	**D0**		**D0**	38
5	**D1**		**D1**	39
7	**D2**		**D2**	40
9	**D3**		**D3**	41
11	**D4**		**D4**	42
13	**D5**		**D5**	43
15	**D6**		**D6**	44
17	**D7**		**D7**	45
19	**D8**		**D8**	46
21	**D9**		**D9**	47
23	**D10**		**D10**	48
25	**D11**		**D11**	49
27	**D12**		**D12**	50
29	**D13**		**D13**	51
31	**D14**		**D14**	52
33	**D15**		**D15**	53
35	**USERDEF0**		USERDEF0	54
37	**WEN**		**WEN**	58
38	**REQ**		**REQ**	59
39	**USERDEF1**		USERDEF1	55
40	**ACK**		**ACK**	60
			USERDEF2	56
			USERDEF3	57

Table 9: SDB/SHB Connectors Pinout comparison

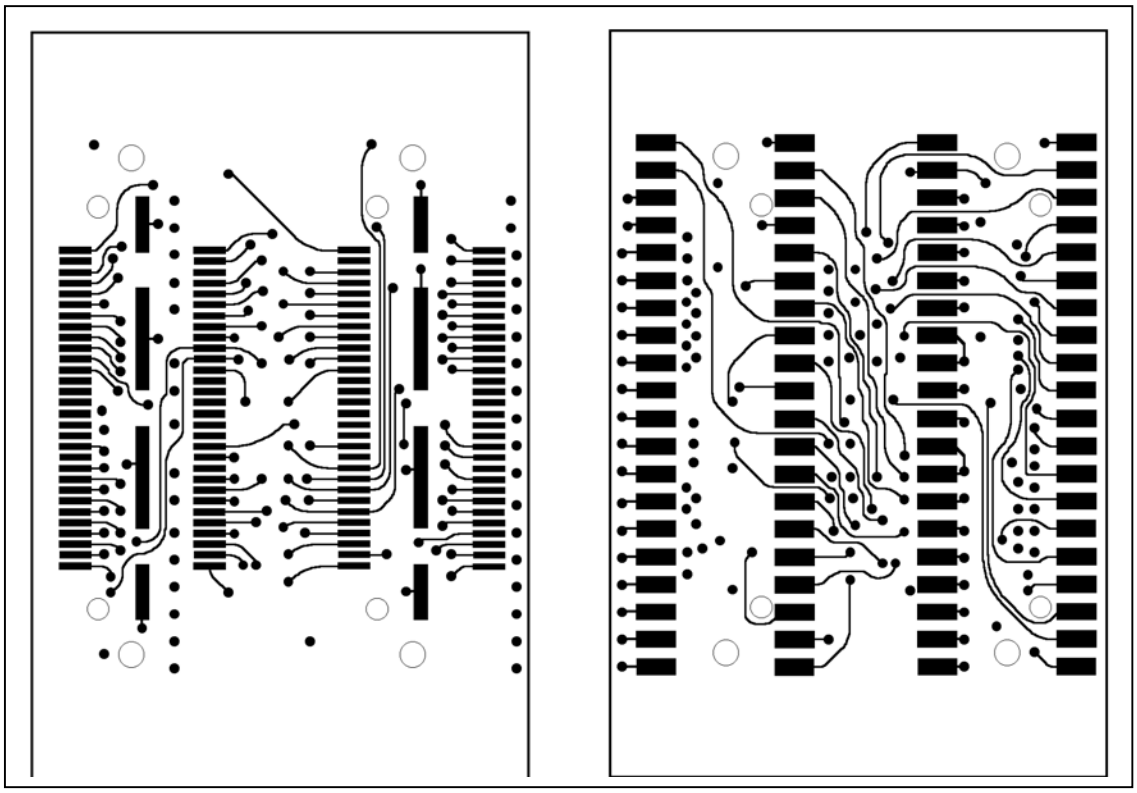

Figure 9: SHB to SDB footprint (Top and bottom)

8 SHB to Front Panel Data Port (FPDP)

8.1 About FPDP:

The Front Panel Data Port (FPDP) is a platform-independent 32-bit synchronous data flow path that allows data to be transfered at high speeds (160 MBytes/sec.) over moderate distances between boards and processing blocks. The FPDP, which is now a widely used standard in the VME world, is expected to quickly become equally popular in the PCI and Compact PCI worlds.

For more detailed explanations, please go to FPDP Web Site. Specifications for the FPDP can be found at: FPDP Specifications.

Standard	FPDP	SHB
Signals Voltage	TTL	LVTTL
Connector Pin count	FPDP-Standard 80 pins used for Unidirectional Interface (See FPDP Specifications)	60 pins
Interface protocol	FPDP protocol	FPDP protocol
Board Connector	KEL Connectors 8831E-080-170L or Robinson-Nugent P50E-080P1-RR1-TG	SAMTEC QSH-60 pins

8.2 FPDP Mezzanine card

A FPDP mezzanine card is necessary to adapt FPDP to SHB.

The mezzanine provides

- Terminations for the transmission lines.
- Drivers/Receivers for Signal Voltage level conversion and performance.
- Mating Connectors

8.3 FPGA Mapping of FPDP

Onboard QSH Conn	FPDP Conn	FPDP pin name	SHB pin name	Onboard QSH Conn	FPDP Conn	FPDP pin name	SHB pin name
1	2	STROB	CLK	31	36	D29	D29
2	79	D0	D0	32	34	D30	D30
3	78	D1	D1	33	33	D31	D31
4	76	D2	D2	34	31	DVALID	WEN
5	75	D3	D3	35	9	DIR	REQ
6	73	D4	D4	36			ACK
7	72	D5	D5	37			CLK
8	70	D6	D6	38	29	SYNC	D0
9	69	D7	D7	39			D1
10	67	D8	D8	40			D2
11	66	D9	D9	41			D3
12	64	D10	D10	42			D4
13	63	D11	D11	43			D5
14	61	D12	D12	44			D6
15	60	D13	D13	45			D7
16	58	D14	D14	46	13	SUSPEND	WEN
17	57	D15	D15	47			REQ
18	55	D16	D16	48			ACK
19	54	D17	D17	49			CLK
20	52	D18	D18	50			D0
21	51	D19	D19	51			D1
22	49	D20	D20	52			D2
23	48	D21/	D21/	53			D3
24	46	D22/	D22/	54			D4
25	45	D23/	D23/	55	17	PIO1	D5
26	43	D24	D24	56	19	PIO2	D6
27	42	D25	D25	57			D7
28	40	D26	D26	58	7	NRDY	WEN
29	39	D27	D27	59			REQ
30	37	D28	D28	60			ACK

Table 10: SHB to FPDP

9 SHB to AGILENT Probe

An adapter is available for Agilent probes for the 16760A Logic Analyser.

The 2 probes supported are the E5378A 100-pin Single-ended Probe and the E5386A Half Channel Adapter with E5378A.

You can find information on the mechanical and electrical specifications of the probe in the User's Guide available from:

http://www.cos.agilent.com/manuals/pdf/16760705.PDF

Also see page 213 of the Help Volume for the 16760A for specifications:

http://www.cos.agilent.com/manuals/help25/help16760.pdf